

1 CLAIMS

2 What is claimed is:

3 1. An apparatus for compensating for glitch occurrence in a
4 reset signal that is applied in an integrated circuit, the
5 apparatus comprising:

6 a logic stage capable to process an incoming signal and a
7 delayed incoming signal that is a delayed version of the
8 incoming signal, the logic stage capable to generate an output
9 signal so that when the incoming signal and the delayed incoming
10 signal are in the same state, the output signal will be in the
11 same state.

16 2. The apparatus of claim 1 wherein the logic stage comprises
17 an S-R flip flop.

18 3. The apparatus of claim 1 wherein the logic stage comprises:

19 a NAND gate capable to receive the incoming signal and the
20 delayed incoming signal;

21 a NOR gate capable to receive the incoming signal and the
22 delayed incoming signal; and

23 an inverter communicatively coupled to the NOR gate and
24 capable to invert an output NOR gate signal from the NOR gate.

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26 4. The apparatus of claim 1 wherein the logic stage comprises:

1 a NAND gate capable to receive the incoming signal and the
2 delayed incoming signal; and

3 an OR gate capable to receive the incoming signal and the
4 delayed incoming signal.

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6 5. The apparatus of claim 1 wherein the delayed incoming
7 signal is delayed by a delay stage.

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6. The apparatus of claim 1 wherein the logic portion is
capable to filter at least one of a first glitch occurring
before a high state portion of the incoming signal and a second
glitch occurring after the high state portion of the incoming
signal.

7. A method of compensating for a glitch in an incoming signal
used for resetting an integrated circuit, the method comprising:

17 receiving an incoming signal;

18 delaying a glitch occurrence in an incoming signal into a
19 delayed incoming signal;

20 performing a logic operation on the incoming signal and the
21 delayed incoming signal; and

22 generating an output signal so that when the incoming
23 signal and the delayed incoming signal are in the same state,
24 the output signal will be in the same state.

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2 8. The method of claim 7, further comprising:

3 applying the generated output signal as a reset signal to
4 at least some portion of an integrated circuit.

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6 9. The method of claim 7 wherein the generating the output
7 signal comprises:

8 filtering at least one of a first glitch occurring before a
high state portion of the incoming signal and a second glitch
occurring after the high state portion of the incoming signal.

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10. An apparatus for compensating for glitch occurrence in a
reset signal that is applied in an integrated circuit, the
apparatus comprising:

11 a logic stage capable to process an incoming signal and a
delayed incoming signal that is a delayed version of the
17 incoming signal, the logic stage capable to generate an output
18 signal so that when the incoming signal and the delayed incoming
19 signal are in the same state, the output signal will have a
20 state similar to the state of the incoming signal, and when the
21 incoming signal and the delayed incoming signal are not in the
22 same state, the output signal will have a state similar to a
23 previously sampled state of the incoming signal.

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1 11. The apparatus of claim 10 wherein the logic stage
2 comprises:
3 an exclusive NOR gate; and
4 a pass-through circuit communicatively coupled to the
5 exclusive NOR gate and capable to pass through the incoming
6 signal in response to an output value from the exclusive NOR
7 gate.

12. The apparatus of claim 10 wherein the delayed incoming signal is delayed by a delay stage.

13. The apparatus of claim 10 wherein the logic portion is capable to filter at least one of a first glitch occurring before a high state portion of the incoming signal and a second glitch occurring after the high state portion of the incoming signal.

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18 14. A method of compensating for a glitch in an incoming signal
19 used for resetting an integrated circuit, the method comprising:
20 receiving an incoming signal;
21 delaying a glitch occurrence in an incoming signal into a
22 delayed incoming signal;
23 performing a logic operation on the incoming signal and the
24 delayed incoming signal; and

1 generating an output signal so that when the incoming
2 signal and the delayed incoming signal are in the same state,
3 the output signal will have a state similar to the state of the
4 incoming signal, and when the incoming signal and the delayed
5 incoming signal are not in the same state, the output signal
6 will have a state similar to a previously sampled state of the
7 incoming signal.

15. The method of claim 14, further comprising:

 applying the generated output signal as a reset signal to
 at least some portion of an integrated circuit.

16. The method of claim 14 wherein the generating the output
17 signal comprises:

1 filtering at least one of a first glitch occurring before a
1 high state portion of the incoming signal and a second glitch
17 occurring after the high state portion of the incoming signal.

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